AMENDMENTS TO THE CLAIMS

The following list of claims replaces all prior versions and lists of claims:

Claim 1 (currently amended): A nonvolatile semiconductor storage device comprising:

a memory array configured such that a plurality of nonvolatile semiconductor memory cells capable of storing one-bit information or multi-bit information are individually arranged in a row direction and a column direction, and a plurality of row lines and a plurality of column lines are arranged to select a predetermined memory cell or memory cells from the plurality of memory cells;

a row decoder circuit that selects a part of the plurality of row lines and that selectively provides a selected row line with a voltage level different from that for other row lines; and

a current-path isolating circuit that, in a test mode different ~~form~~ from a normal operation mode, isolates a current path in the device into a first current path for a current flowing through the row line selected and a second current path for a current not flowing through the row line but flowing through the row decoder circuit, the current path isolated being formed for supplying a testing voltage to the selected row line from a testing voltage source.

Claim 2 (original): The nonvolatile semiconductor storage device according to claim 1, further comprising two external connecting pads each for receiving the testing voltage supplied from the testing voltage source, wherein one of the two external connecting pads corresponds to the first current path and the other one of the two external connecting pads corresponds to the second current path.

Claim 3 (original): The nonvolatile semiconductor storage device according to claim 1, wherein:

a rearstage section of the row decoder circuit comprises a plurality of row selection circuits that each apply a predetermined voltage in units of the row line corresponding to a select/unselect state of the row line, the plurality of row selection circuits being each formed of a driver stage and a predriver stage that drives the driver stage;

the first current path is formed for the current flowing through the row line via at least one of a plurality of switching devices and a pullup device of the driver stage, the plurality of switching

devices constituting a mode switch circuit that switches between the normal operation mode and the test mode; and

the second current path is formed for the current flowing through the predriver stage via at least another one of plurality of switching devices.

Claim 4 (original): The nonvolatile semiconductor storage device according to claim 1, wherein the nonvolatile semiconductor memory cells each have a MOSFET structure and concurrently have an information storage structure capable of electrically programming and erasing information into the MOSFET structure.

Claim 5 (original): A row-line short defect detection method for detecting a row-line short defect in a nonvolatile semiconductor storage device comprising:

a memory array configured such that a plurality of nonvolatile semiconductor memory cells capable of storing one-bit information or multi-bit information are individually arranged in a row direction and a column direction, and a plurality of row lines and a plurality of column lines are arranged to select a predetermined memory cell or memory cells from the plurality of memory cells; and

a row decoder circuit that selects a part of the plurality of row lines and that selectively provides a selected row line with a voltage level different from that for other row lines,

the row-line short defect detection method comprising the step of, in a test mode different from a normal operation mode, isolating a current path in the device into a first current path for a current flowing through the row line selected and a second current path for a current not flowing through the row line but flowing through the row decoder circuit, the current path isolated being formed for supplying a testing voltage to the selected row line from a testing voltage source.

Claim 6 (original): The row-line short defect detection method according to claim 5, wherein, in the step of isolating, the testing voltage is isolated into two testing voltages to be supplied from a testing voltage source to two external connecting pads and supplied from the testing voltage source, wherein one of the two external connecting pads corresponds to the first current path and the other one of the two external connecting pads corresponds to the second current path.

Claim 7 (original): The row-line short defect detection method according to claim 5, wherein a rearstage section of the row decoder circuit comprises a plurality of row selection circuits that each apply a predetermined voltage in units of the row line corresponding to a select/unselect state of the row line, the plurality of row selection circuits being each formed of a driver stage and a predriver stage that drives the driver stage,

wherein, in the step of isolating:

the first current path is formed for the current flowing through the row line via at least one of a plurality of switching devices and a pullup device of the driver stage, the plurality of switching devices constituting a mode switch circuit that switches between the normal operation mode and the test mode; and

the second current path is formed for the current flowing through the predriver stage via at least another one of plurality of switching devices.

Claim 8 (original): The row-line short defect detection method according to claim 5, wherein the semiconductor memory cells each have a MOSFET structure and concurrently have an information storage structure capable of electrically programming and erasing information into the MOSFET structure.